

Vayu/J6 8-Layer Reference Design Study Read Me Notes

June 26, 2017

The J6 Digital Radio Infotainment (DRI) Reference Design Study consist of SCH and PCB design source files. The SCH shows the core components (i.e. J6 SoC, single SoC PMIC, 2 banks of DDR3L & high-speed SERDES interfaces) required for a J6 class product. The 8-layer, controlled impedance PCB design illustrates how to apply Low Density Interconnect (LDI) & IPC Class2 design rules needed for a low cost PCB. The PCB design shows core component placement, 100% signal breakout, high-speed SERDES & matched DDR data byte group signal routing, Power Distribution Network (PDN) routing with optimal Decoupling Capacitor (Dcap) schemes that meet all recommended Power Integrity (PI) parameters for key SoC power rails. Taken together, these design source files will enable a customer's design team "to jump start" their end product designs.

Please be aware this J6 8-Layer Reference Design Study is a design optimization study only and no PCB is planned to be built. The 16-layer EVM PCB has been built & tested. The EVM board has been designed to support SoC silicon testing and software development. As a result, more signaling traces, breakout connectors & SoC ball multiplexing switches are needed than an end product requires. All EVM PCB key design elements (controlled impedance, DDR3 & high-speed signal routing, robust PDN, ...) have been included into this simplified 8-layer reference PCB design. The Ref Design Study has achieved very good results in illustrating SCH & PCB simplification vs EVM design that can be shared with key customers on an "As Is" basis. The Ref Design Study SCH & PCB source are consider to be "Work-In-Progress" (WIP) since occasional design updates may occur in order to include improvements and enhancements.

The J6 Automotive PCB Design Rules presentation provides a summary of possible PCB design parameters that could be used to produce a low cost, low density interconnect (LDI), IPC Class2 type automotive PCB. Each customer should review & understand how PCB design parameters can affect PCB manufacturability and their end product's use cases, environmental ranges & reliability goals.

The J6 Power Integrity Analysis & Dcap Optimization summary report shows how optimizing a PCB's Power Distribution Network (PDN) can lead to optimizing Dcap schemes for each unique PCB design (i.e. power routing, component placement, via placement, Dcap footprint interconnections). Conducting PI analysis during PCB design is recommended in order to ensure each PCB design meets recommended PI parameters for robust processor operation while using the least number of Dcaps per power rail. Ultimately, less Dcaps means less vias resulting in more signal routing channels for interfacing to J6 SoC which is key for reducing PCB layers & cost.

The following list captures the present status of known "improvement opportunities" with the current J6 Ref Design Study PCB design:

1. There are a few "DDR data signal stubs" that could be improved to show "a more optimal" DDR3 Fly-By Routing example. Present routing is same as done on J6 EVM PCB.

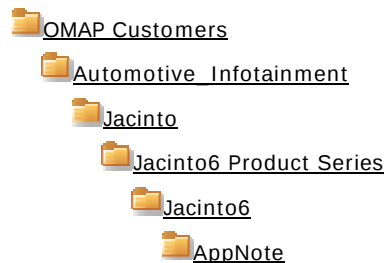
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2. Further optimizing of DDR3 and other key high-speed signal (i.e. HDMI, PCIe, USB3, QSPI, SD/MMC) routes are planned for sometime in 1Q 2014. In the meantime, one can use the Vayu EVM's RevF PCB source file or "Vayu PCB High Speed Routing Reqs v0p3" pdf file as a reference for high-speed signal routing.

You can find the latest J6 DRI Reference Design Study SCH & PCB source files along with all support documents on CDDS per the folder path & links shown below.

CDDS Folder Path & Links:



Unmanaged Data - Vayu 8-Layer Reference Design-1.2:

US - <https://cdds.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.36616.13595>

India - <https://cdds-india.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.36616.13595>

France - <https://cdds-nice.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.36616.13595>

Japan - <https://cdds-japan.ext.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.36616.13595>

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US Design Zone/ODC - <https://cdds-dz.itg.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.36616.13595>

India Design Zone/ODC - <https://cdds-india-dz.itg.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.36616.13595>

France Design Zone/ODC - <https://cdds-nice-dz.itg.ti.com/ematrix/common/emxNavigator.jsp?objectId=28670.42872.36616.13595>